Design Enablement, Flows, and Services

TSMC 2011 Technology Symposium

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New DFR – SER Simulation Solution

- SER (Soft Error Rate) Trend: As technology scaling down, chip level SER is increasing, and logic SER is catching up with SRAM bit SER
- SER simulation is to support product design optimization and time-to-market without compromising product quality
- TSMC SER Simulation Solutions
  - Technology: 40nm, 28nm
  - Device SER Characterization: eSRAM, eDRAM, Flip-Flops
  - Process SER Response Model
  - 3rd Party Simulation Service (iRoC): Cell/Lib FIT, Circuit SER
  - SER Testing: High Energy Neutron, Thermal Neutron, Alpha Particle
- Applications Mainly Concerned by SER
  - High End Computing (Banking, Stock Exchange, E-commerce)
  - High End Networking (Data Center Switches & Routers)
  - Automotive (Anti-Brake Systems, Stability Control)
  - Biomedical (Pacemakers)

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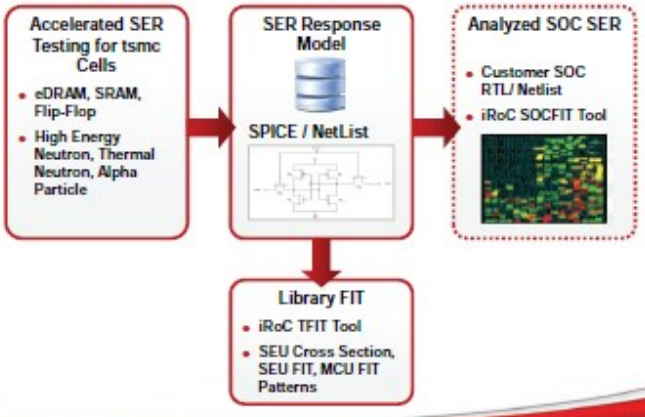
TSMC SER Simulation Flow



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