SUCCESS STORIES

« SOCFIT is a comprehensive tool which embeds the complexity of analyzing reliability issues on very large SoC designs. The complexity of the problem is that many sources of errors can affect the reliability of the chip. SOCFIT helps quantify these issues and points to the areas of the design that need to be improved. The tool is helpful to explain our design's reliability performances to our customer in a clear and quantitative way. IROC experts have been very helpful and flexible in the deployment of this tool and its companion tool TFIT within LSI.»

Miguel VILCHIS Reliability engineer

LSI Corporation designs, develops and markets complex, high-performance storage and networking semiconductors and storage systems. It provides silicon-to-system solutions that are used at the core of products that create, store, consume and transport digital information. The company offers a broad portfolio of capabilities, including custom and standard product integrated circuits used in hard disk drives, solid state drives, high-speed communications systems, computer servers, storage systems and personal computers. It also offers external storage systems, storage systems software, redundant array of independent disks, or RAID, adapters for computer servers, and RAID software applications. The company operates through two segments: Semiconductor and Storage Systems. The company was founded on November 6, 1980 and is headquartered in Milpitas, CA.

The Challenge:

LSI uses the latest process nodes to fulfill the demanding needs of its customers, among which are the larger players in the Cloud infrastructure industry. The soft error challenge posed by this type of application is multiple: not only the quantity of SoC in server and storage farms is rapidly increasing, raising the statistical likelihood of SER occurrence, but also chips are becoming more complex (larger number of cells), faster, denser and running at lower voltages. All these elements combined make the risk of SER occurrence per chip higher as well. With strong limitations on power and area budget per design, LSI had to come with a pro active way to meet requirements for SER performance and other specification and even more importantly be able to document the results quantitatively to their customers.

The Solution:

IROC and LSI worked on a multi faceted approach to answering this question. The first step had been to conduct a detailed pilot project involving the analysis of one of LSI large designs by IROC's SOCFIT tool. The benefit of this approach is for LSI to learn more about the capabilities of the tool and how it can be used internally. To IROC engineer, the project was a way to learn the internal EDA environment at LSI as they had to adapt SOCFIT to exchange data with already installed design and simulation environment. SOCFIT was then adopted by LSI together with its companion tool TFIT. TFIT allows LSI to predict soft error FIT rates of their individual cells and then build a SER database which is an important input to SOCFIT simulation. In order to run accurate TFIT prediction, LSI obtained from their foundry access to the response model that characterizes the specific process node to ionizing particles impacts. In the process of deploying the SOCFIT platform at LSI, IROC had the chance to train LSI engineers, optimize the tool for LSI environment and support LSI in the presentation of this SER predictive capability to their end customer.

The Results:

SOCFIT and TFIT are now deployed at LSI's central R&D which is now presenting this new capability to each business unit involved in developing SoC in need of SER analysis and mitigation strategy. Eventually, the TFIT and SOCFIT licenses are used by a number of business units for almost every new design start, which will lead to better design, on time delivery and customers convinced that the chip won't fail them during lifetime of their router or storage unit.

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