



White Paper

**New Trends and Solutions
To Combat Soft Error Threats
To
Nanometer Semiconductors**

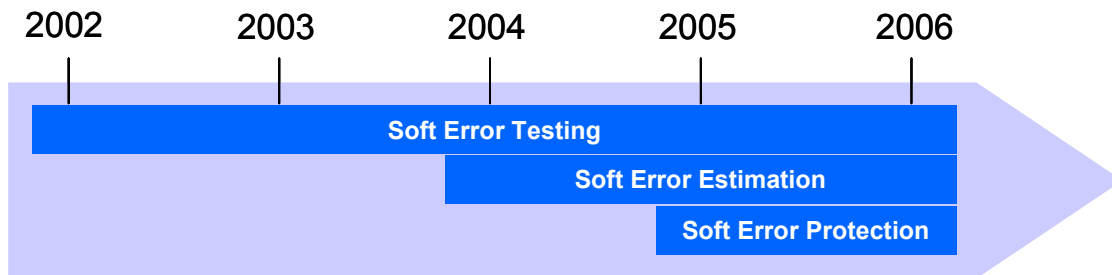
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New Trend in the Soft Error Threat

Reliability is one of the major concerns for advanced semi-conductor manufacturers. Soft errors induced by alpha particles and atmospheric neutrons are among these concerns. By hitting the transistors, such particles may cause unpredictable bit flips in ICs (integrated circuit). To quantify the sensitivity of their chips to soft errors, it becomes necessary for chip manufacturers to run radiation testing on their latest IC generation. But today the trend goes beyond only measuring the soft errors. People want now to be able to estimate the soft error rate during the design phase in order to do something about it before sending the circuits to production. And the ultimate step against the soft error threat is the protection against it: implementing some circuitry during the design cycle to eradicate the reliability issues due to these particles. This article presents this trend and details these different phases.



Soft Error Characterization Trend

Soft Error Testing

Most IC manufacturers are sensitive to the soft error threat and a real need for radiation testing is identified. iRoC Technologies developed a turn key service solution called SERTEST™ that allows customers to get the soft error rate, the conditions in which they occur (voltage, data pattern) and the type of error generated (single bit, multibit, upset) for any IC including memories, FPGA's , and SoC's (System on Chip). Since 2002, iRoC tested more than 100 device types in 20 test campaigns. Major_IDMs (Integrated Device Manufacturers), Fabless Companies and Foundries such as Toshiba, Netlogic and TSMC chose to perform radiation tests with iRoC in multiple test facilities in the US and in Europe. While in 2002 only the volatile memories seemed to be sensitive to soft error, in 2003 iRoC tested Flash, FPGAs and even SoC for several chip manufacturers. Logic cores and FPGAs are known to be much less sensitive to soft errors than memories but with the operating frequency increasing, the geometry shrinking, and the power supply reduction tend to drastically raise the soft error sensitivity of these devices. As a networking SoC provider leader states, "We start getting some issues with the configuration registers of our network processor."



Since these registers are set at the beginning of the operation and remain unchanged during the whole use cycle, they become sensitive as well. In 2004, the trend will move toward testing any types of IC. This is confirmed by the high level of customer demand for iRoC radiation test service in 2004.

Soft Error Estimation and Simulation

In 2004, chip manufacturers will not only run radiation testing but now also will need to be able to predict the soft error rate for their ICs. It is really the next step of the soft error assessment process. The designer should be able to estimate the soft error rate during the design cycle in order to do his best to decrease the soft error sensitivity before sending the chip to production. iRoC is developing a product line of design solutions called SERFIT™ that allow the designer to estimate his IC soft error rate during the design phase, without any radiation testing. This methodology takes into account the effect of soft errors in the memories, the registers and the combinational logic. For the memories, it considers failure probability per memory unit (Failure In Time (FIT) per bit). For the register, it is based on the same probability: the failure per registers. For the logic gates, the methodology is more complex since it takes into account the probability of a transient error occurrence into a combinational gate as well as the pulse width of the current transient generated by the particle. These two parameters will be used by SERFIT Products to analyze the propagation of the errors into the combinational logic network. SERFIT Products will run logic simulations and computation based on these different parameters. Based upon the product type and the level of complexity, the SERFIT Products will provide an estimate of the soft error rate for the given IC.

Soft Error Protection

Tests and estimation are not enough for some chip designers. Projecting forward into 2005, people will continue testing their chip under radiation, estimating the soft error rate during the design cycle, but for devices that have mission critical applications, like network routers, telephony base stations, the soft error rate must be optimized and reduced to an acceptable level. The designs will need protection against soft errors in order to produce reliable products. Many memory integrators already implement some Error Correcting Codes (ECC) but they still need more efficient solutions in terms of performance and area overhead and the size of memory grows. Likewise, chip manufacturers also seek solutions for their FPGAs and their SoC that contains not only memories but also combinational logic. The iRoC SERPRO™ Professional Services Teams offer customized solutions to implement soft error protections in SoC's and Memories then ensure the right level on soft error protection is design in with as little impact as possible to the other design variables such as area, power, and speed.. These solutions are based on iRoC's proprietary ECC implementations for memories and "just right" redundancy for logic cores.

The ultimate step is then to implement protection techniques to ensure an acceptable level of robustness against soft error. From radiation testing services to IC protection techniques through soft error estimation tools, iRoC Technologies will provide its expertise, products and design services to the semiconductor industry.



The iRoC Competitive Advantage

Many high-end IC providers are now being required by their customers to get soft error data and in some cases even to propose and or implement a soft error protection solution. These companies could choose to develop the internal knowledge on soft errors and try to understand the nuclear physics, the resultant effects at transistor level, at design level, and at system level. It would require the need to hire a dedicated team of soft error specialists and also engage and manage the various beam facilities... But few semiconductor companies decide to dedicate teams to carry out soft error testing or to investigate what is the soft error effect on their products. These activities cost far too much in terms of resources and time. At iRoC, we have developed the expertise and methodology in concert with the JEDEC standard and validated by over 100 soft error campaigns and over 1000 analysis efforts. In addition, we are an independent provider focused only on soft error issues. By selecting iRoC, companies are getting an independent qualification of their soft error results.

Conclusion

Reliability and in particular soft errors are becoming an issue as design and systems move into nanometer processes. Initially, soft errors were considered a threat only for people integrating a huge number of memories into their systems. But nowadays, many memory, FPGA and SoC providers run radiation testing to quantify the sensitivity of their products to soft errors. And the trend for the next few years will be to go much further by running soft error estimations during the design phase to avoid unreliable products. As one of the largest independent providers of soft error solutions iRoC Technologies, is ready to ensure the semiconductor industry is able to successfully combat the soft error threat.