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## **iRoC SELLS MEMORY BIST DIVISION TO SYNOPSYS**

### **iRoC to Expand Leadership Role in Soft Error Protection**

**SANTA CLARA, Calif. – Mar. 15, 2004** - iRoC Technologies, a leading provider of solutions for semiconductor soft error protection, announced today it has sold its Memory BIST Division to Synopsys, Inc. The sale includes an exclusive patent license for sales and marketing of M-BISTeR™, plus full ownership of software source code for product maintenance and ongoing development. Memory BIST (Built-in Self Test) is a convenient way to test embedded memories on system-on-Chip (SoC) devices. Initially developed in TIMA labs, iRoC's M-BISTeR is an electronic design automation (EDA) tool that offers unique features such as low-cost programmability and BIST sharing to support SRAM, ROM and Dual Port SRAM memories. Financial details were not released.

iRoC developed memory BIST to capitalize on a mature market need, but decided to sell its BIST division to Synopsys, the leading provider of EDA software for integrated circuit (IC) design and verification.

“We are particularly proud that the leader in EDA chose iRoC Memory BIST solutions,” stated Eric Dupont, CEO and president of iRoC Technologies. “This best-in-class technology is a perfect match for the needs of many EDA customers today. iRoC's soft error solutions are dedicated to high performance chips, nanometer process and high-end applications. This sale gives iRoC the means to sharpen our products and extend our expertise as the leading provider of solutions to free ICs from soft error risk.”

The potentially harmful effect of soft errors is widely recognized and the industry is moving toward a global solution for a SoC platform encompassing embedded memories, IP cores and libraries. iRoC embraces all SoC platform needs with three product lines:

- SERTEST™ for Soft Error Rate testing of ICs and FIT rate qualification on silicon;
- ROBAN™ for FIT rate estimating at the RT level of the SoC design phase;
- RoCKIT™ for protecting and embedding fault tolerant solutions into SoC.

With more than 20 customers, SERTEST, iRoC's radiation test service, has established the leadership position in qualifying memories and SoC versus Failure In Time (FIT) rate due to alpha particles and atmospheric neutrons. Field test results provide evidence that occurrences of soft errors are increasing for nanometer technologies and more complex SoCs. SERTEST's internal data base is an extensive means toward developing the next technology methodology for soft error sensitivity prediction.

In 2004, the first market segments demanding FIT reduction solutions are critical applications such as networking, telecommunication and transportation. System houses are squeezing their chip providers to reduce the FIT rate from several thousand per chip to as low as a few hundred per chip. Using iRoC's expertise in soft errors, designers are able to get a clear and accurate vision of the feasibility and the most cost-effective methodology to meet the market's desired FIT specifications. Later this year, iRoC plans to release new soft error simulation capabilities that will apply to all SoC components and provide an accurate FIT estimation.

### **About iRoC Technologies**

iRoC Technologies develops and licenses design fault tolerant solutions and test services to enhance the security, quality and reliability of nanometer integrated circuits. More information on the company's products and services can be obtained at [www.iroctech.com](http://www.iroctech.com).

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