Event Information

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REVIEW of iRoC at IRPS 2004

SANTA CLARA Calif. — May 3, 2004 — iRoC Technologies actively participated in the 42nd annual International Reliability Physics Symposium, April 25 - 29, by showing at its booth its Soft Error Testing service which:

- Provides a turn key solution for testing any type of IC
- Provides customers with in depth analysis of all types of failures detected during the test
- Follows the industry standard and is recognized and adopted by major semiconductor companies

iRoC also showed the features of it Soft Error Assessment technology which:

- Takes care of Nuclear physics for designers
- Performs risk analysis, allowing assessment early in the design phase
- Gives functional FIT rate, not worst case
- Walks the designer through the process of improving the design for better FIT

"At iRoC we have solutions for radiation testing and are developing products for SER prediction and IC protection from soft errors," said Olivier Lauzeral, vice president for

operations at iRoC Technologies. “The effect of technology shrinking affects not only the sensitivity of memory cells to single event upsets, but also creates new effects to be looked at, such as Multi Bit Upset (MBU), Single Event Functional Interrupt (SEFI) and micro Latch up. One should check not only the memory cells but also the access logic in its investigation to measure or assess the FIT rate.”

Besides the well recognized effects on memories, soft errors spread also in logic devices for mission-critical systems such as servers, automotive ICs and networking equipment. Chip designers are looking closely at the logic parts of their IC on ways to guard against the effects of cosmic rays and alpha particles emitted from packaging, to meet the requirements of their system customers.

Hans Stork, chief technical officer of Texas Instruments, delivered the keynote address, stating that reliability concerns "are at the very center" of the chip industry. His presentation explained how new failure modes threaten as the industry moves to new materials and to complex system-on-chip solutions with multiple device types on the same die. The keynote talk inferred that more attention needs to be paid to soft error rates (SER), which grow more important as memory blocks on SoCs grow in size. Errors, caused in part by cosmic rays striking SRAM cells, are becoming an issue for logic as well.

About 600 engineers attended the 2004 IRPS. During the week a full set of tutorials covering the essentials of semiconductor reliability were presented. Tutorial tracks covered advanced topics in reliability; including future trends in CMOS, gate dielectrics, low-k/Cu interconnect systems, RF/MMIC reliability, and failure analysis. Over 95 technical papers were presented. As last year, a session was specifically dedicated to Soft Errors effects; with the international on-line testing symposium, IRPS is likely to become the event that best addresses the Soft Error problem.

About iRoC Technologies

iRoC Technologies develops and licenses design soft error solutions and test services to enhance the security, quality and reliability of nanometer integrated circuits. More

information on the company's products and services can be obtained at www.iroctech.com.

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