



## NEWS RELEASE

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### **iRoC Technologies Introduces Free Web-based Tool for Soft Error Risk Assessment of Integrated Circuits**

*Company to Demonstrate New Soft Error Analysis Tool at October 6<sup>th</sup> FSA Suppliers Expo*

**SANTA CLARA Calif. — October 4, 2004** —iRoC Technologies<sup>®</sup> Corporation introduced the Soft Error Analysis Web Tool, a new web-based tool that assesses the Soft Error Risk (SER) of integrated circuit (IC) designs. The company will demonstrate the tool on October 6<sup>th</sup> in booth 202 at the 2004 FSA Suppliers Expo ([www.fsa.org/suppliers\\_expo/](http://www.fsa.org/suppliers_expo/)), at the San Jose McEnery Convention Center in San Jose, Calif. The online tool will also be available at [www.iroctech.com](http://www.iroctech.com) on that date. iRoC is one of the world's leading commercial providers of soft error solutions for ICs.

The Soft Error Analysis Web Tool enables design and quality engineers and managers to assess the risks of soft errors—transient faults caused by external radiation that affect the logic states of ICs and memories—in their systems-on-chips (SoCs), application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), or memories. The tool also gives recommendations on steps that can be taken to quantify and also reduce the soft error failure-in-time (FIT) rate if the target application or industry requires it.

“Soft errors pose increasingly higher risk to IC designs as the industry moves to lower process geometries, the memory block sizes increase, and more of the information handled by today’s devices is viewed as mission critical,” said Michael Buehler-Garcia, iRoC’s vice-president of marketing.

“Designers must find out now if their design is at risk so they can begin taking real steps to avoid the critical failures soft errors can cause. The Soft Error Analysis Web Tool is a first-of-its-kind educational tool that helps determine this risk so designers can achieve their reliability targets.”

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### **Soft Error Analysis Web Tool Leverages iRoC's Deep Soft Error Knowledge**

The Soft Error Analysis Web Tool is based on iRoC's vast store of statistical data on soft error sensitivity that it has accumulated from multiple efforts using its test vehicles, 3D simulations, and soft error protection services. The Tool analyzes user input on chip size, process node, targeted process, amounts of memory and logic, type of memory, and target application or market. It then processes the soft error rate estimation, maps it against a RISK scale, and gives the user information on the SER failure in time (FIT) risk for that design in various market scenarios.

### **Pricing and Availability**

iRoC's Soft Error Analysis Web Tool can be accessed for free on iRoC's website at [www.iroctech.com](http://www.iroctech.com) as of October 6, 2004, and will be demonstrated on that date at the 2004 FSA Suppliers Expo. Attendees who view a demonstration at the conference will receive a French walking stick from iRoC.

### **About iRoC Technologies**

Founded in 2000, privately-held iRoC Technologies Corporation is one of the world's leading commercial providers of soft error solutions for integrated circuits. iRoC provides soft error testing, soft error optimization tools, and soft error protection services that help semiconductor companies estimate the reliability risks of soft errors and eliminate them during the chip design process. Caused by atmospheric radiation, soft errors are the fastest growing reliability problem for semiconductors. iRoC's U.S. headquarters are in Santa Clara, Calif, and its European headquarters are in Grenoble, France. Visit [www.iroctech.com](http://www.iroctech.com) for the latest news and information on iRoC.

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