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Kit helps chip developers to avoid 'soft-error' blues

[Richard Goering](#)

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DESIGN TOOLS

Santa Cruz, Calif. - Radiation-induced "soft errors" are becoming a hard problem for chip designers at 90 nanometers and below. Soft-error testing firm Iroc Technologies Corp. this week will roll out what it calls the first commercial tool to analyze a design for sensitivity to soft errors.

Soft errors-transient faults caused by neutrons or alpha particles-have long plagued memory designers and, as feature sizes decrease, are now starting to affect logic designers as well.

Using neutron beams from one of four qualified sites, [Iroc](#) runs postproduction qualification tests, but they aren't cheap.

To help chip designs minimize the problem in the first place, Iroc's SoCFIT tool set takes Verilog gate-level netlists and predicts the failure-in-time (FIT) rate for each block in the design. An FIT is one soft error per 10^9 hours per device.

Increasingly, networking and storage systems are demanding a low FIT rate, said Eric Dupont, Iroc's president and CEO. And no wonder. A transient failure could corrupt data or even crash a system, he said. "We know of maybe four or five cases where people realized a soft error was the cause of a field failure," he said.

To create SoCFIT, Iroc took its internal Serfit software and broke it in two, said Michael Buehler-Garcia, vice president of marketing and business development at Iroc. One piece is a transistor-level tool to be introduced this March. The other is SoCFIT, which works at a gate level.

SoCFIT allows a system-on-chip designer with a standard-cell library "to look at bit rates by hierarchical block and by memory block," Buehler-Garcia said."

SoCFIT runs about as fast as synthesis tools, he said, so a small block could run in a few minutes. The tool can do full-chip analysis. SoCFIT will be available in the first quarter starting at \$10,000.

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