TFIT ™ 2.0

Transistor Level Soft Error Analysis

Assess Your Soft Error Risk During Design

OVERVIEW:

In nanometer designs, soft errors have become as issue that must be considered during the design phase. An accurate and fast simulation method is needed for users who have the ability to modify the cell design (IDMs, libraries developers) or for foundries interested into improving the Soft Error immunization of their technology (90nm and below). This tool is necessary to predict and improve the SER performance of their design before production.

TFIT allows assessment of the soft error threat of design at the transistor level, early in the design flow at much faster speeds that traditional 3D TCAD simulations and equivalent accuracy. Furthermore, TFIT can be customized to the users' technology just like internal TCAD effort, and can integrate correlation with silicon test results.
Using the TFIT software and models provided by iRoC, designers can quickly quantify device soft error sensitivity. With that knowledge, standard cell libraries and memory cells soft error sensitivity can be modified to match the targeted reliability of the design.

KEY ATTRIBUTES	BENEFITS
Fast and accurate Soft Error Analysis	Fast simulation time compared to 3D TCAD Efforts (cycle time of days vs. months)
	Very little drop in accuracy vs. 3D TCAD thanks to TFIT Models leveraging iRoC soft error expertise (test correlation and nuclear database)
Customized to the users' technology	Provides soft error sensitivity assessment for memory and logic cells libraries cell
	Specific process models are custom built by iRoC experts for a real user specific tool
Plugs Seamlessly into Design Flow	TFIT interoperates with most popular SPICE Engines
	Uses designers functional test benches, no additional test benches required

T-FIT 2.0 IN THE DESIGN FLOW

The Designers' **inputs** are:

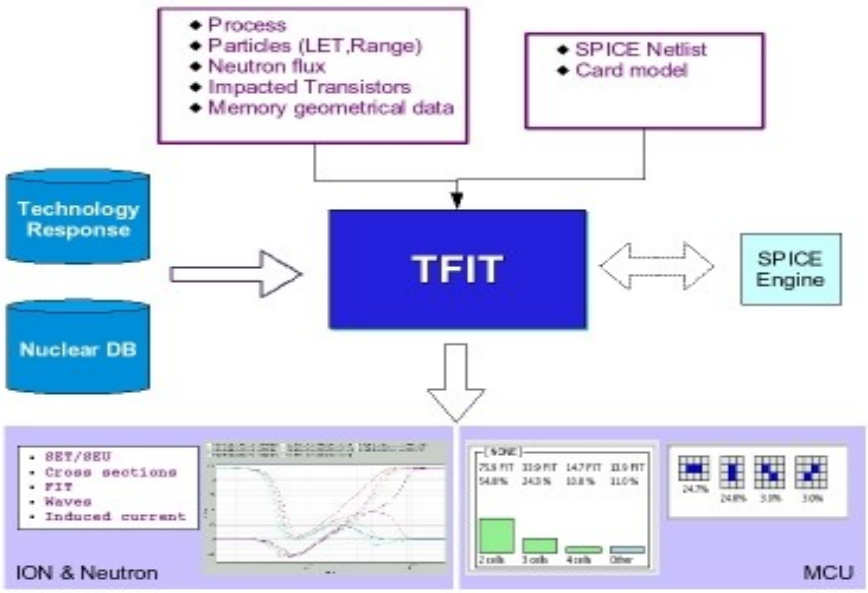
- The design description: SPICE **netlist** of the target block and the card model
- The radiation environment to consider: **Neutron** (user-defined energy) or **Ions** (LET values)
- User defined simulation parameters: Process, impacted transistors, spice simulator

From these inputs, TFIT calls the soft error models developed by iRoC for the target technology to generate current pulses for the specified environment. It then injects this current pulse into the design netlist during transistor level simulation.

Depending on computation mode, TFIT **outputs** are:

- The single particle impact effects, in particular **cell flip** in case of memorizing structure
- The **current pulse curves** induced by particle impacts (neutron & ion cases)
- The per-transistor **FIT value** (neutron case)
- **Cross-section** calculation of each transistor (ion case)
- The MCU's FIT values and their physical patterns in the memory (MCU case)

Depending on the sensitivity shown by the target block, the Designer can then elect to modify the design to change the effect of soft error according to the target application.



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