



## NEWS RELEASE

### FOR IMMEDIATE RELEASE

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## **iRoC Technologies Introduces TFIT Software to Help Custom and Handcrafted Chips Meet Reliability Targets**

*Newest Product in iRoC's Soft Error Design Solution Platform  
Analyzes Soft Error Strikes at Transistor Level*

**D.A.T.E. CONFERENCE, MUNICH, GERMANY — March 7, 2005 — iRoC Technologies®**

Corporation, one of the world's leading commercial providers of soft error solutions for integrated circuits (ICs), introduced TFIT™ software, the newest product in its Soft Error Design Solution Platform. TFIT lets IC designers analyze the impact of soft error strikes on their custom designs to help meet reliability targets. Soft errors are transient faults caused by external radiation—mainly cosmic rays—that affect the logic states of ICs and memories.

“For nanometer designs, reliability, and in particular soft error analysis, is no longer just a process issue,” said Jim Hogan, general partner, Telos Venture Partners. “Growth in the amount of embedded memory and the lower activation energies of nanometer processes increase the risk of system reliability issues due to soft error strikes. Because soft errors can't be eliminated using classic reliability techniques, they must be addressed during the design phase. ASIC and fabless companies are now feeling pressure from end customers to provide soft error probabilities, and they are turning to their foundries and IP vendors for help in addressing this. As such, the industry needs soft error solutions like those being offered by iRoC.”

“Soft error concerns have traditionally been the purview of the military and aerospace industries because of the mission critical nature of those applications,” said Michael Buehler-Garcia, iRoC's vice president of worldwide marketing and business development. “Today, the data in commercial applications such as storage systems and network routers carry data that is also considered mission critical to end customers. This now makes soft errors a concern for memory designers, network processor designers, and IDM library development teams targeting these markets. For designers working at the transistor and SPICE netlist level, TFIT provides valuable insight into the soft error sensitivities of design blocks, in cycle times that are much faster than other soft error approaches.”

**TFIT Delivers Soft Error Capabilities to Designers with Interoperability and Speed**

Currently, TCAD/3D modeling techniques are used for SPICE level soft error analyses. However, since TCAD/3D systems do not focus specifically on soft error issues, to accurately model a single strike/single angle is at least an overnight run, and full soft error analysis of a memory or IP block could take weeks. In contrast, by leveraging iRoC's soft error models, TFIT can do the same simulations in seconds, and full soft error analysis of an IP block in several days.

In addition, designers do not need to develop any additional tools or scripts to use TFIT, which is fully interoperable with SPICE simulators, allowing a true design change feedback loop scenario.

After TFIT extracts the IP block or part of the design to be analyzed, the designer selects the location where he'd like to simulate a strike, and TFIT performs analysis using the designer's test bench and iRoC's proprietary soft error models. TFIT provides the results in tabular form or as a current curve displayed on the designer's SPICE simulator. This enables the designer to determine if a certain type of strike at a particular place in the design will cause a state change—such as a logic or bit flip—in his IP. TFIT will also output a statistical “bucketized” profile of soft error probabilities, which will tell the designer to what types of strikes his design is most sensitive.

The designer can either select default modes or select specific activation energies and strike angles, to further understand the sensitivity of a design. Based on the analysis, the designer can make changes to the design, such as changing the length and width of the transistor level design, to reduce the soft error sensitivity. Designers can then re-run the analysis to see if the same type of strike still causes a state change.

**iRoC's Soft Error Expertise Reduces Risk for Designers**

iRoC's soft error modeling techniques are derived from expertise in soft errors both at the nuclear reaction level and from over 1,000 soft error testing efforts. From this expertise, iRoC has developed TFIT and the other products in its Soft Error Design Solution Platform to give designers the ability to make accurate trade-offs with tools that interoperate with their design flow, while shielding them from the underlying complex nuclear physics of soft error analysis. The first product in the Platform—the SoCFIT™ software solution that analyzes the soft error risk of a system-on-chip (SoC) at full chip and block level—was announced in January.

Together, the products allow designers to understand the soft error risk and sensitivities of their design, IP block or library before it is released to production—in contrast to today's approach of knowing only after the finished product has been tested in a neutron beam facility. Having this knowledge up front means that transistor and SPICE level designs can be soft error hardened, reducing their sensitivity to soft errors during design.

Likewise, developers of standard cell libraries and memory bit cells can use TFIT to design soft error hardened variants of bit cells and standard cells that are much less sensitive to soft errors. SoC designers can then select these soft error hardened elements for those portions of their design that need more soft error protection, resulting in SoCs that are less sensitive to soft errors.

### **Availability**

TFIT will be available to the general market in Q2 2005. For more information, contact iRoC Technologies by email at [sales@iroctech.com](mailto:sales@iroctech.com), or visit [www.iroctech.com](http://www.iroctech.com).

Attendees of DATE 2005 ([www.date-conference.com](http://www.date-conference.com)), being held in Munich, March 7 – 11, 2005, can view a demo of both products in iRoC's Soft Error Design Solution Platform in iRoC's booth, number C5100. A member of Cadence Design Systems, Inc.'s Connections<sup>®</sup> program, iRoC will demo TFIT with the Cadence<sup>®</sup> Virtuoso<sup>®</sup> Spectre<sup>®</sup> Circuit Simulator.

### **About Cadence Connections Program**

The Cadence Connections program promotes open interoperability in all areas of electronic design including digital, custom IC, analog/mixed-signal and PCB design. By attracting best-in-class partners, Cadence offers the industry's largest collection of third-party solutions operating fully with the Cadence suite of design tools. The Connections program has over 130 member companies working toward developing an optimized silicon design chain for customers. Information about the Connections program may be found at [www.cadence.com/partners/connections/](http://www.cadence.com/partners/connections/).

### **About iRoC Technologies**

Founded in 2000, privately-held iRoC Technologies Corporation is one of the world's leading commercial providers of soft error solutions for integrated circuits. iRoC provides soft error testing, soft error optimization tools, and soft error protection services that help semiconductor companies estimate the reliability risks of soft errors and eliminate them during the chip design process. Caused by atmospheric radiation, soft errors are the fastest growing reliability problem for semiconductors. iRoC's U.S. headquarters are in Santa Clara, Calif, and its European headquarters are in Grenoble, France. Visit [www.iroctech.com](http://www.iroctech.com) for the latest news and information on iRoC.

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