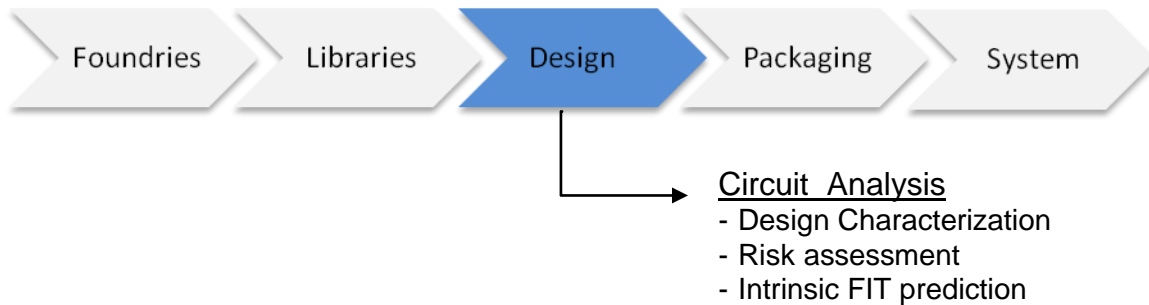


SoCFIT System Level Soft Error Analysis



OVERVIEW

In latest semiconductor nodes, the system sensitivity to Soft Error Rate (SER) is getting worse as transistors scale and systems integrate more and more silicon. Memories are not the only sensitive parts contributing to SER, but logics are playing a significant role at 65nm and beyond.

The SER is becoming a part of system reliability with a need to define clear metrics and to identify the causality between a SER in a component and its effect on the whole system.

A systematic approach for identifying these connections requires the usage of dedicated tools to link raw cell SER to circuit SER, to System SER and eventually to user SER.

iRoC Technologies developed the SoCFIT tool platform as a prediction and analysis tool linking raw cell SER to circuit SER and System SER.

For ASIC designers who need to accurately assess the Soft Error Rate performance of their pre-silicon design, SoCFIT is a comprehensive simulation tool platform that accounts for the different types of de-ratings in an explicit way and with good accuracy.

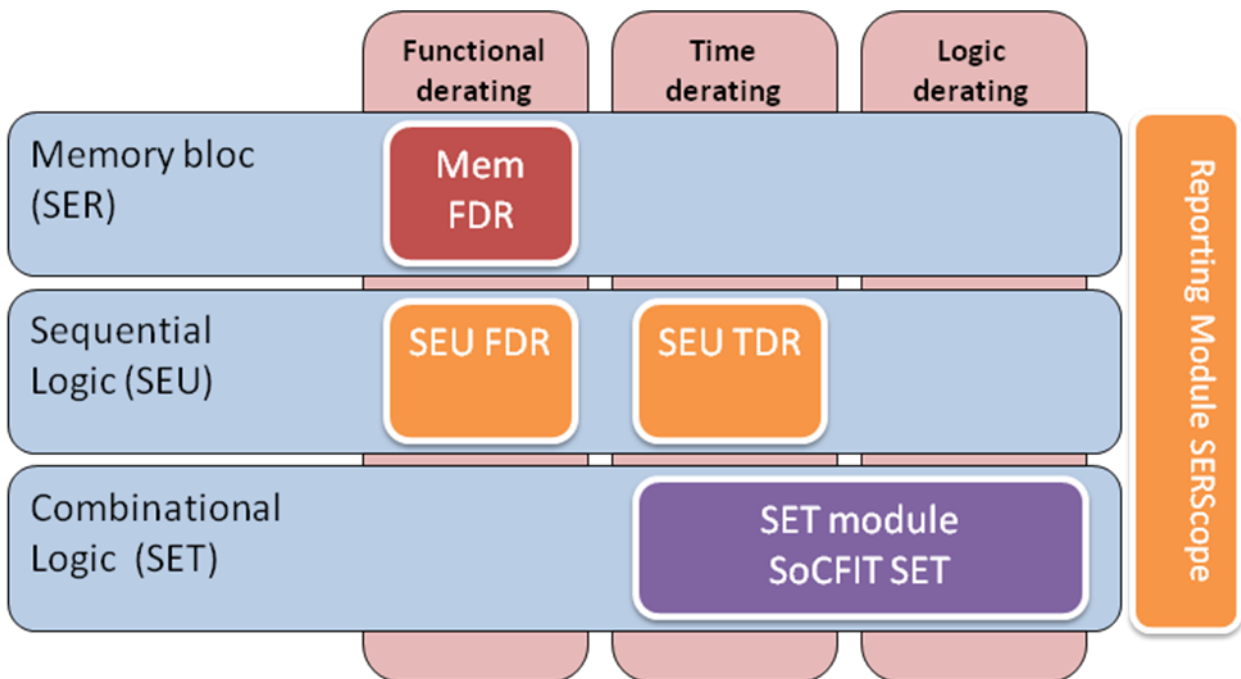
Based on this expertise, designers using SoCFIT can identify which area of the design contributes mostly to the FIT and therefore can modify the architecture of the circuit to improve its resilience to soft errors and its overall reliability.

SoCFIT Key Benefits

FEATURES	BENEFITS
Gate Netlist or RTL input	Decisions for silicon resource allocation budget, need to be made very early in the design phase. RTL definition of the circuit allows it.
Includes different types of de-rating	Logic, timing and application specific masking affect widely the results. SoCFIT offers a clear control of these de-ratings for accurate risk management
Leverage our experience in Soft Error on different generations of silicon	Users don't need to build an extensive soft error expertise but will still get the best support and results.
Deliver tool with professional quality and support	Users can include the tools in their design flow with confidence for long term support.

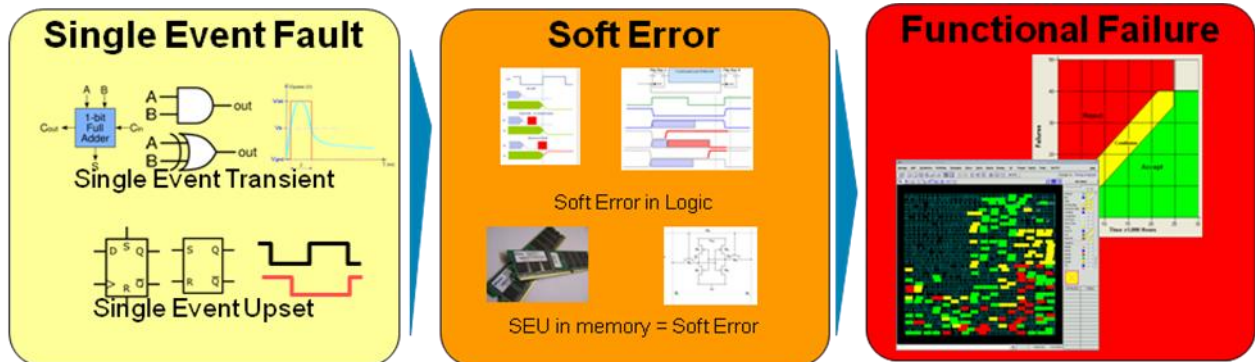
SoCFIT :ARCHITECTURE AND ECOSYSTEM

SoCFIT presents a modular architecture according to the need of the user. The standard module is the SEU module (sequential module) including the reporting module. To this can be added the Memory bloc module and the combinational Logic module.



SoCFIT is an EDA tool that computes the FIT of a circuit by taking into account the intrinsic sensitivity (cross-section) of each feature of the circuit (cell instances, memory blocks, IPs, black boxes etc..) multiplied by de-rating factors. The intrinsic sensitivity of each feature is retrieved from a database (called the Soft Error Rate Database).

SoCFIT uses either the RTL definition of the circuit, or the gate level Netlist, and timing files. It analyses Same Clock cycle propagation and Many Clock cycles propagation as described below, to determine the derating factors.



Single Event Fault ► Soft Error

(Same Clock Cycle Propagation)

- **Logic De-rating:** logic propagation from the output of the affected cell to the inputs of a sequential cell or memory
- **Temporal De-rating:** an estimation of the opportunity window

Soft Error ► Functional Failure

(Many Clock Cycles Propagation)

- **Functional De-rating:** logic propagation from the output of the affected cell to the inputs of a sequential cell or memory

INPUT NEEDED FOR A CIRCUIT SIMULATION

- SER database for the process node. This is a database of cells used in the design and their corresponding SER performances. This is either build using TFIT® tool, or shared by the foundry (provided the user is using the foundry's standard cells). Missing information for proprietary cells for example can be added to the SER database by the user at any time (open format database).
- Circuit RTL or gate level Netlist
- Timing files (for Netlist analysis)



DATA SHEET

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