



NEWS RELEASE

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iRoC Technologies Introduces Soft Error Design Solution Platform

First Product, SoCFIT, Provides Designers with Soft Error Analysis Capability to Reduce Risk

SANTA CLARA Calif. — January 24, 2005 —iRoC Technologies® Corporation, one of the world's leading commercial providers of soft error solutions for integrated circuits (ICs), introduced its Soft Error Design Solution Platform to help IC designers meet reliability targets. The first product in the Platform—the SoCFIT™ software solution—analyzes the soft error risk of a system-on-chip (SoC) at full chip and block level, giving designers insight into which blocks may be the major contributors to the over all soft error rate (SER), and enabling them to perform trade-off analyses between various design elements to meet their targets. SoCFIT helps reduce risk for designers by providing the soft error failure-in-time (FIT) range during the design phase instead of in a post-production qualification test—where the cost of failures can be prohibitive. Soft errors are transient faults caused by external radiation—mainly cosmic rays—that affect the logic states of ICs and memories.

“At 90 nanometers and below, soft errors increasingly affect both memory and logic elements of a design,” said Yervant Zorian, chief scientist at Virage Logic and vice president of the IEEE Computer Society. “Soft errors are becoming a challenge in meeting IC reliability targets today for critical products in the networking and telecom markets. Since soft errors can't be screened with classical test techniques such as at-speed testing and burn-in, they must be addressed during the design phase—making reliability a design issue.”

“We are hearing from more and more ASIC and fabless companies that their customers are starting to ask about soft error risk, and in general these companies are having a hard time answering the questions,” said Eric Dupont, iRoC's president and CEO. “With SoCFIT, we are offering for the first time a commercially-available product that allows designers to analyze the soft error risk and sensitivities of their design before it is released to production. This is in sharp contrast to today's approach of knowing only after the finished product has been tested in a neutron beam facility.”

With the high cost of chip design, companies can't risk failing a qualification test. The designer must know his soft error risk during design, when he has a chance to fix it. SoCFIT is just the first product in iRoC's Soft Error Design Solution Platform that will help automate the prediction and ultimately the eradication of soft errors.

Soft Error Design Solution Platform Leverages iRoC's Deep Soft Error Expertise

Understanding how soft errors are induced by cosmic rays, alpha particles and thermal neutrons is extremely complex. To accurately project the risks requires knowledge of both nuclear physics and semiconductor devices. iRoC's soft error modeling techniques are derived from expertise in soft error both at the nuclear reaction level and from over 1,000 soft error testing efforts. iRoC's Soft Error Design Solution Platform leverages these techniques, distilling the complex issues into a solution that provides accurate data to the designer within his current design flow.

SoCFIT Enables Designers to Determine Soft Error Rate and Perform Trade Offs

SoCFIT fits into industry standard design flows by accepting Verilog gate level netlists. Designers do not need to learn or develop any additional tools or techniques to use it. Once a designer has a preliminary design that meets timing and power constraints, a copy of the design can be output to SoCFIT, which then analyzes it against iRoC's soft error models for the target process and library. This model-based analysis speeds results, since multiple scenarios can be addressed in a shorter time.

Based on constraints set by the designer, SoCFIT outputs soft error figures of merit, which are organized according to a designer-defined block hierarchy, including each memory element. When designers can see what the soft error rate is and which design blocks are the largest contributors, they can determine the criticality of the data being transmitted over those blocks, and perform tradeoff analyses. Designers can then implement techniques such as redundancy, error correction coding (ECC) or hardened cells to reduce the soft error risk to an acceptable level.

SoCFIT features an easy to use GUI and flexible command line controls. A graphical output interface allows plotting of FIT results for each module.

Availability

SoCFIT will be available to the general market in Q1 2005 with industry generic models for 130nm. For more information, including pricing, contact iRoC Technologies by email at sales@iroctech.com, or visit www.iroctech.com.

Attendees of DesignCon 2005 (www.designcon.com) can view a demo of the product in iRoC's booth (number 726) at the show, being held January 31 through February 3, 2005.

About iRoC Technologies

Founded in 2000, privately-held iRoC Technologies Corporation is one of the world's leading commercial providers of soft error solutions for integrated circuits. iRoC provides soft error testing, soft error optimization tools, and soft error protection services that help semiconductor companies estimate the reliability risks of soft errors and eliminate them during the chip design process. Caused by atmospheric radiation, soft errors are the fastest growing reliability problem for semiconductors. iRoC's U.S. headquarters are in Santa Clara, Calif., and its European headquarters are in Grenoble, France. Visit www.iroctech.com for the latest news and information on iRoC.

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