



NEWS RELEASE

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iRoC Technologies Introduces SERPRO Services for Transistor-level Soft Error Rate Analysis and Optimization

*Determining the Fast-growing Risk of Soft Errors During
Integrated Circuit Design Increases Reliability*

SANTA CLARA Calif. — October 6, 2004 —iRoC Technologies® Corporation introduced its SERPRO™ services for transistor-level Soft Error Rate (SER) prediction and optimization. The services help semiconductor companies perform faster and more accurate soft error modeling before design tape out—making their integrated circuits (ICs) more reliable in the field. Soft errors are transient faults caused by external radiation—mainly cosmic rays—that affect the logic states of ICs and memories. iRoC is one of the world's leading commercial providers of soft error solutions for ICs.

“With the significant increase in overall chip development costs, semiconductor companies need to know ahead of going into production what their Chip SER is projected to be,” said Eric Dupont, iRoC’s president and CEO. “Up to 90 nanometers, both standalone and embedded memories have been the primary design element impacted by cosmic rays, so memory providers and designers of SoCs with large memory elements will benefit greatly from our new services. As more devices are designed for 90nm and 65nm nodes, potential damage from cosmic rays will not only affect memory elements, but also logic gates. Designers of memory and logic devices need to be able to analyze, simulate, predict and optimize their SER numbers during the design cycle to achieve their target SER rate and ensure product reliability.”

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“Soft-error solutions are becoming essential to achieving IC reliability targets for critical products—and increasingly for mainstream consumer products—as soft errors become more prevalent,” said Handel Jones, president and CEO of IBS, Inc., a leading semiconductor consultancy firm. “Companies like iRoC that offer combined predictive and testing solutions that leverage the continuous learning based on years of testing, will be critical in how successful the semiconductor industry is in dealing with the soft error issues.”

SERPRO Transistor-level Services Offer Choices for SER Analysis and Optimization

iRoC’s SERPRO transistor-level services leverage iRoC’s soft error optimization techniques, database of global radiation information, soft error test chips, and SERTEST™ soft error qualification testing solutions. The services are based on iRoC’s soft error model development methodology, and are targeted for design and quality engineers working on designs at the transistor level.

Customers can choose from two distinct transistor-level services. With the first, iRoC provides to the customer soft error models in the form of SPICE model curves—generated by neutron or alpha particles hitting the device. These models give customers access to unequalled analysis speed, reducing simulation time from months to days, with a very high level of accuracy. This SERPRO service allows designers to simulate soft error scenarios in developing custom memories, bit cells, and standard cell library elements. The second service gives the customer guaranteed soft error optimization. With this service, iRoC collaborates with an IC design team to establish a design’s current soft error failure-in-time (FIT) rate, then guarantees achievement of an improved FIT rate if the changes recommended by iRoC are incorporated. Included in this service is a SERTEST shuttle slot to qualify the final product for soft errors.

With both services, designers get transistor simulations for soft error sensitivity that are significantly faster than other 3D or TCAD efforts. The services are customized so they are flexible, providing the exact level of support needed by the customer.

Pricing and Availability

iRoC’s SERPRO transistor-level services are now in beta testing and will be available to the general market in Q1 2005. For pricing information, contact your local sales office or email sales@iroctech.com. For more information, visit www.iroctech.com.

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About iRoC Technologies

Founded in 2000, privately-held iRoC Technologies Corporation is one of the world's leading commercial providers of soft error solutions for integrated circuits. iRoC provides soft error testing, soft error optimization tools, and soft error protection services that help semiconductor companies estimate the reliability risks of soft errors and eliminate them during the chip design process. Caused by atmospheric radiation, soft errors are the fastest growing reliability problem for semiconductors. iRoC's U.S. headquarters are in Santa Clara, Calif, and its European headquarters are in Grenoble, France. Visit www.iroctech.com for the latest news and information on iRoC.

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