

FOR IMMEDIATE RELEASE

For More Information:
Olivier Lauzeral
iRoC Technologies
408-982-9994
olivier.lauzeral@iroctech.com

IROC LAUNCHES ITS PROFESSIONAL SERVICE FOR SOFT ERROR RISK-FREE DESIGNS

SERPRO™ assists design centers match upcoming SER specifications from System Houses with a team of experts combined with a unique toolbox.

SANTA CLARA, Calif. – February 7th, 2006 - iRoC Technologies, one of the world's leading commercial providers of soft error solutions for integrated circuits (ICs), announced today its SERPRO™ services for SoC designs. More than one year after its transistor-level SER simulation service introduction, SERPRO™ now leverages iRoC test service, simulation tools, process characterization and design experience to help design centers build solutions for SER issues brought by nanometer processes. "Today system houses issue soft errors specifications for applications addressing broader markets such as networking, automotive or medical devices. We experience now more SER specific requests from design centers than ever", stated Eric Dupont, CEO of iRoC Technologies. "In most cases, SER expertise to assess soft errors risks and to elaborate a plan for SER mitigation is what our clients are lacking". With SERTEST™, the well-recognized SER testing service and award winning TFIT™, an advanced tools for process and library characterization, SERPRO delivers the best-in-class expertise on SER threat understanding, lowers the cost of SER analysis, and helps build a consistent SER mitigation strategy.

iRoC's drivers for offering this service to the industry stem from new dilemma felt by IC designers when asked by their client to address the problem of radiation-induced soft errors or latch up. After timing, power and yield, it is a brand new piece of the design matriochka that creates new burden on design team.

How serious is this problem? Which evidence should I show my customers to convince them that my design is SER-risk free? How to address this problem within area and

power budget? How to measure the SER on my silicon? These are questions that SERPRO service helps answer.

SER analysis can be run at each phase of the design flow from RT Level to die: “If the cost to fix designs for SER is 1X at RT Level, it will be 10X at die level and 100X after shipment” added Dupont. “With design and masks costs increase, these ratios will get one order of magnitude higher for 65nm and below”.

Addressing SER early in the design phase is the only way to allocate the smallest area and power for Soft Error protection. Our SERPRO simulation tools help evaluate the right budget avoiding costly overprotection by fixing only the hot spots of the design that need to be improved.

In an iterative process, our experts team up with our customer’s team to check SER performance all along the design process and to provide design architecture solutions for SER protection. SERPRO adopters are also able to run the toolkit flow themselves at their site.

The last step of the project is usually the silicon SER qualification test “We predict beam time allocation issues this year”, states Olivier Lauzeral, GM of the radiation test Business Unit at iRoC, “with the growing demand from the industry and diminishing supply of qualified neutron beam time worldwide, we will soon face a shortage problem.” SERPRO adopters will benefit from the iRoC yearly Test Shuttle Program and will have a better visibility on their product SER qualification possibilities.

SERPRO experts will design the experiment to bring the most appropriate SER qualification test results at device level or at full-system level to match the RAS (Reliability, Availability and Serviceability) strategy of system houses. “We offer customers the most qualified particles sources that fit their application needs. To achieve this, we run 8 to 10 test campaigns a year in more than four different labs worldwide,” explains Lauzeral.

SERPRO team also helps write analysis reports, present test results, and explain to the end customer the effort carried out to solve the issue. Because iRoC Technologies is an independent third party player, which focus only on solving the soft errors and latch up

issues, its experts will give an un-biased and candid report of the soft error threat for any design.

Come and visit us at Designcon 2006 (Booth 715) to learn more about our Soft Error solutions.

About iRoC Technologies

Founded in 2000, privately-held iRoC Technologies Corporation is one of the world's leading commercial providers of soft error solutions for integrated circuits. iRoC provides soft error testing, soft error optimization tools and soft errors professional services that help semiconductor companies eliminate the reliability risks of soft errors during the chip design process. Caused by atmospheric radiation, soft errors are the fastest growing reliability problem for semiconductors. More information on the company's products and services can be obtained at www.iroctech.com.

iRoC Technologies SERTEST™ and SERPRO™ are registered trademarks of iRoC Technologies Corporation.

###